Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-5. (Canceled)

6. (Currently amended) A method for preventing electrostatic damages to integrated circuit elements of a semiconductor chip package during storage, the package having a plurality of terminals connected to the integrated circuit elements, the method comprising:

forming one or more conductive members electrically connecting the terminals to each other, thereby short-circuiting the terminals so that voltage is not applied to the integrated circuit elements of the semiconductor chip package before it is mounted on a printed circuit board; and

disabling the electrical connections by an action of mounting the package on a printed circuit board, wherein the electrical connections are melted by a heat of soldering the terminals so that operation of the semiconductor chip package is not obstructed.

7. (Original) The method of claim 6, wherein the step of forming the conductive members comprises forming solder members connecting the terminals, and wherein the action of mounting the package comprises soldering the terminals.

8. (Original) The method of claim 7, wherein the step of forming the conductive members comprises forming solder lines connecting the terminals.

9. (Currently amended) The method of claim 7, wherein the step of forming the conductive members comprises forming a conductive thin film on surfaces of the terminals, areas between the terminals and peripheral areas of a bottom surface of the package.

10-11. (Canceled)

12. (Previously presented) The method of claim 9, wherein the step of forming the conductive thin film comprises patterning the conductive thin film by a photolithography process and an etching process.

13. (Currently amended) The method of claim 8, wherein the solder lines are formed to a net-like structure, such that each of the terminals is connected to other of the terminals by multiple electrical paths.

14. (Currently amended) The method of claim 8, wherein the solder lines are formed to a single line-like solder member, such that each of the terminals is connected to other of the terminals by a single electrical path.

15. (Canceled)

16. (New) A method for preventing electrostatic damages to integrated circuit elements of a semiconductor chip package during storage, the package having a plurality of pin-shaped terminals connected to the integrated circuit elements, the method comprising:

forming one or more wires electrically connecting tip-portions of the pin-shaped terminals to each other, thereby short-circuiting the terminals so that voltage is not applied to the integrated circuit elements of the semiconductor chip package before it is mounted on a printed circuit board; and

cutting the wires by an action of inserting the terminals into sockets of a printed circuit board to eliminate the short-circuited state of the terminals so that operation of the semiconductor chip package is not obstructed.

17. (New) The method of claim 16, wherein the wires are gold wires.

18. (New) The method of claim 17, wherein the gold wires have a thickness of approximately 70 μm.

19. (New) The method of claim 16, wherein the wires are fixed to the terminals by an ultrasonic pressure bonding method.